

Fig. 1

# Multi-Symbol Signaling Technique

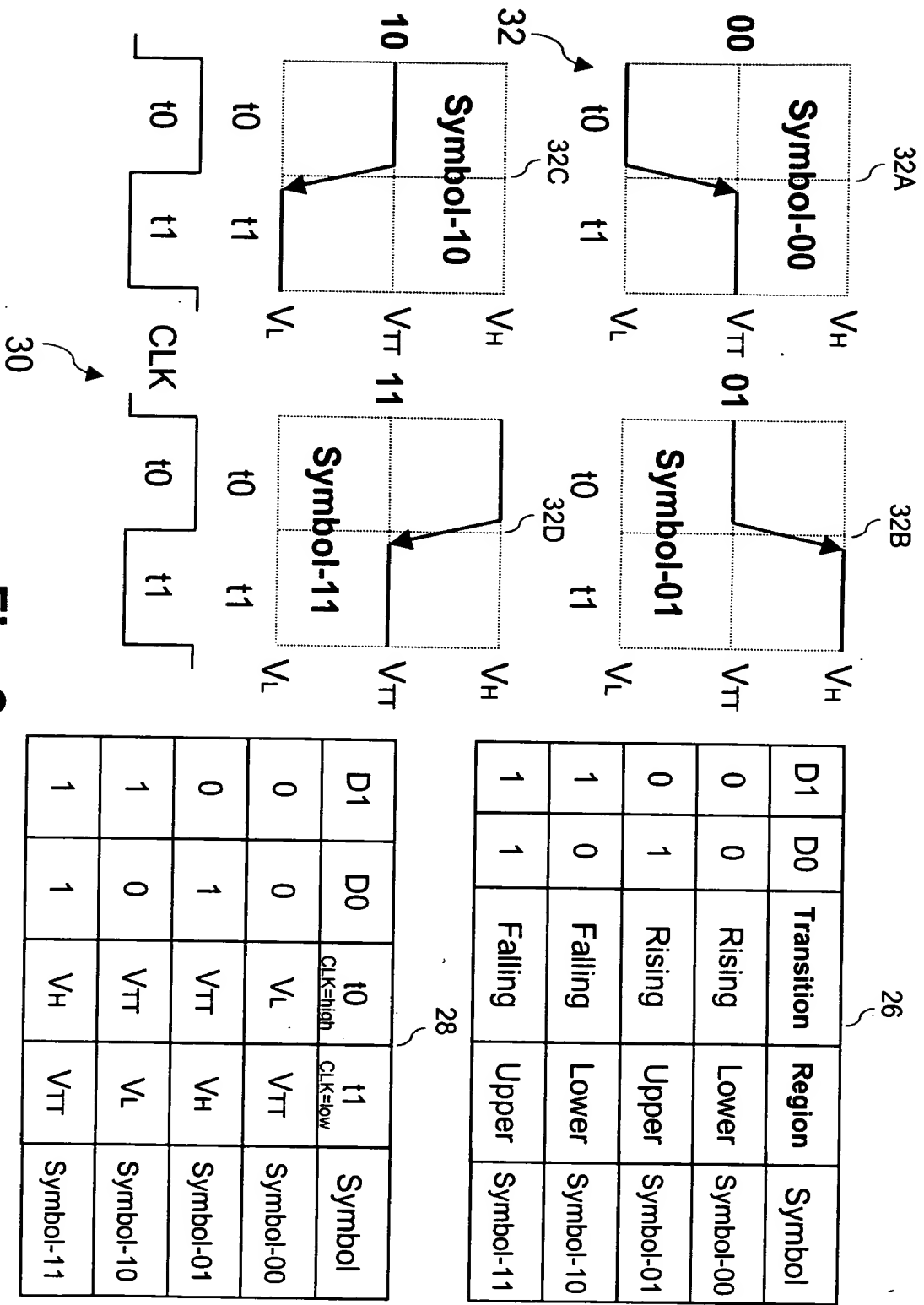


Fig. 2

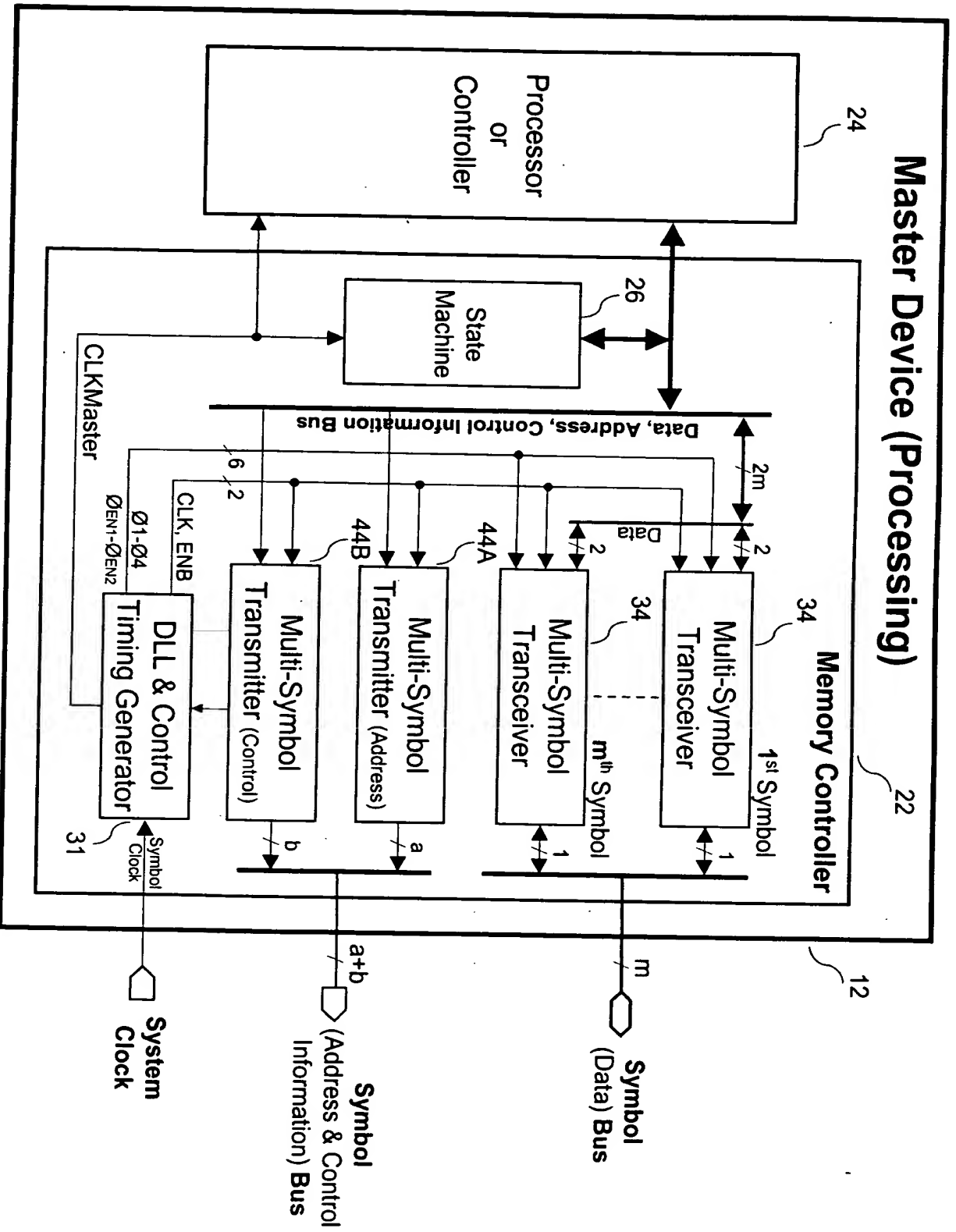
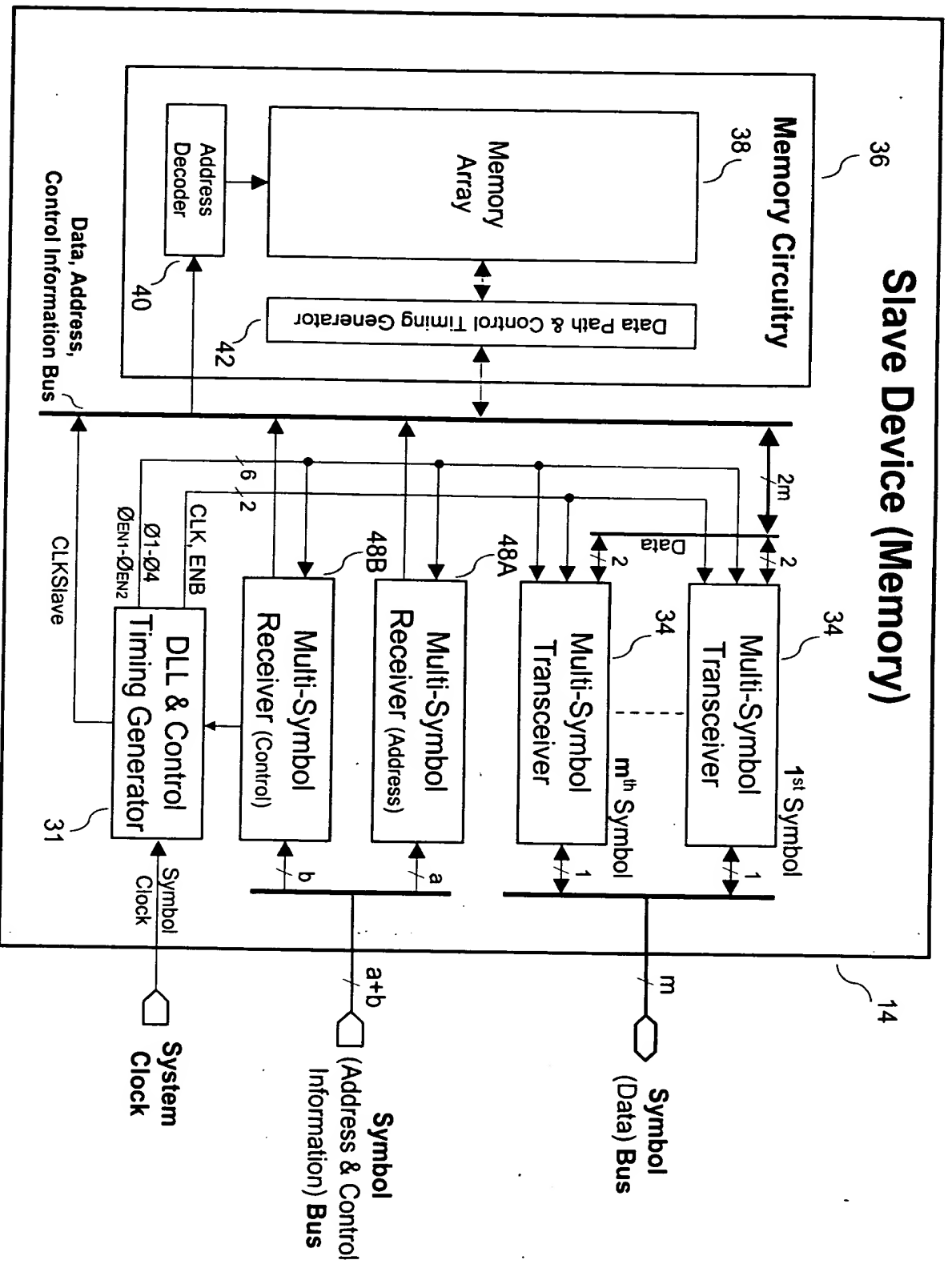
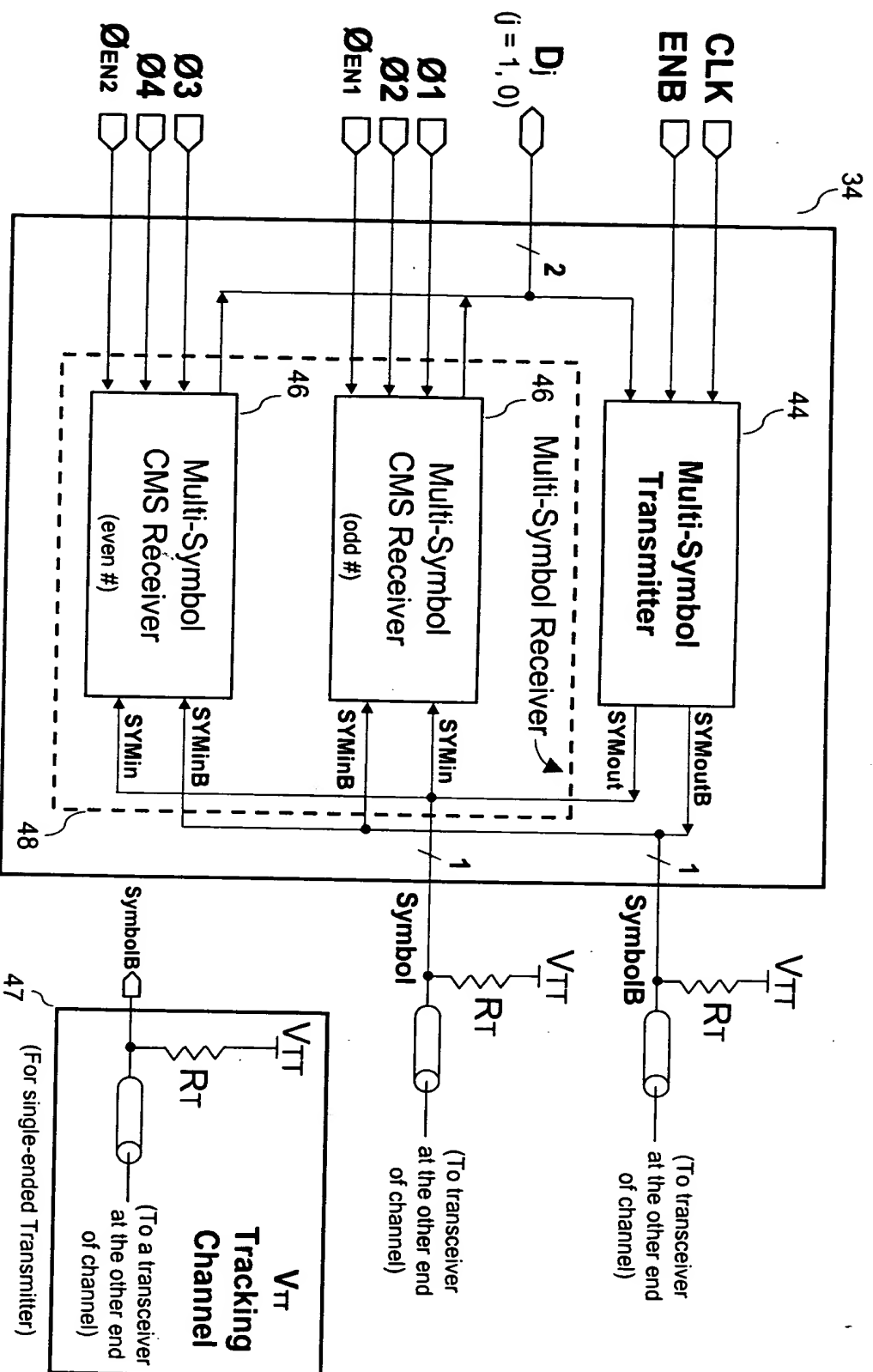


Fig. 3



**Fig. 4**

# Multi-Symbol Transceiver



**Fig. 5**

Figure 1 illustrates a Multi-Symbol Transmitter and Receiver system. The transmitter (44) includes a Multi-Symbol Encoder Circuit (56) and a Driver Strength Control Circuit (54). The encoder circuit receives data inputs D0 and D1, and a clock input CLK. It outputs control signals do0 and do1 to the driver strength control circuit. The driver strength control circuit then controls a differential output stage (50) consisting of PMOS (51) and NMOS (53) transistors. A supply source (55) and a level calibration circuit (52) are connected to the output stage. The receiver (14) consists of Slave Device-1 and Slave Device-k connected to a bus (44) with a resistor (RT) to VTT. Timing parameters t0 and t1 are indicated for the signal transitions.

	D1	D0	t0 CLK=high	t1 CLK=low
	0	0	V <sub>L</sub>	V <sub>TT</sub>
	0	1	V <sub>TT</sub>	V <sub>H</sub>
	1	0	V <sub>TT</sub>	V <sub>L</sub>
	1	1	V <sub>H</sub>	V <sub>TT</sub>

	$t_0$ CLK=high	$t_1$ CLK=low
D1	D0	
0	0	$V_L$
0	1	$V_{TT}$
1	0	$V_L$
1	1	$V_H$

# Multi-Symbol Transmitter (differential)

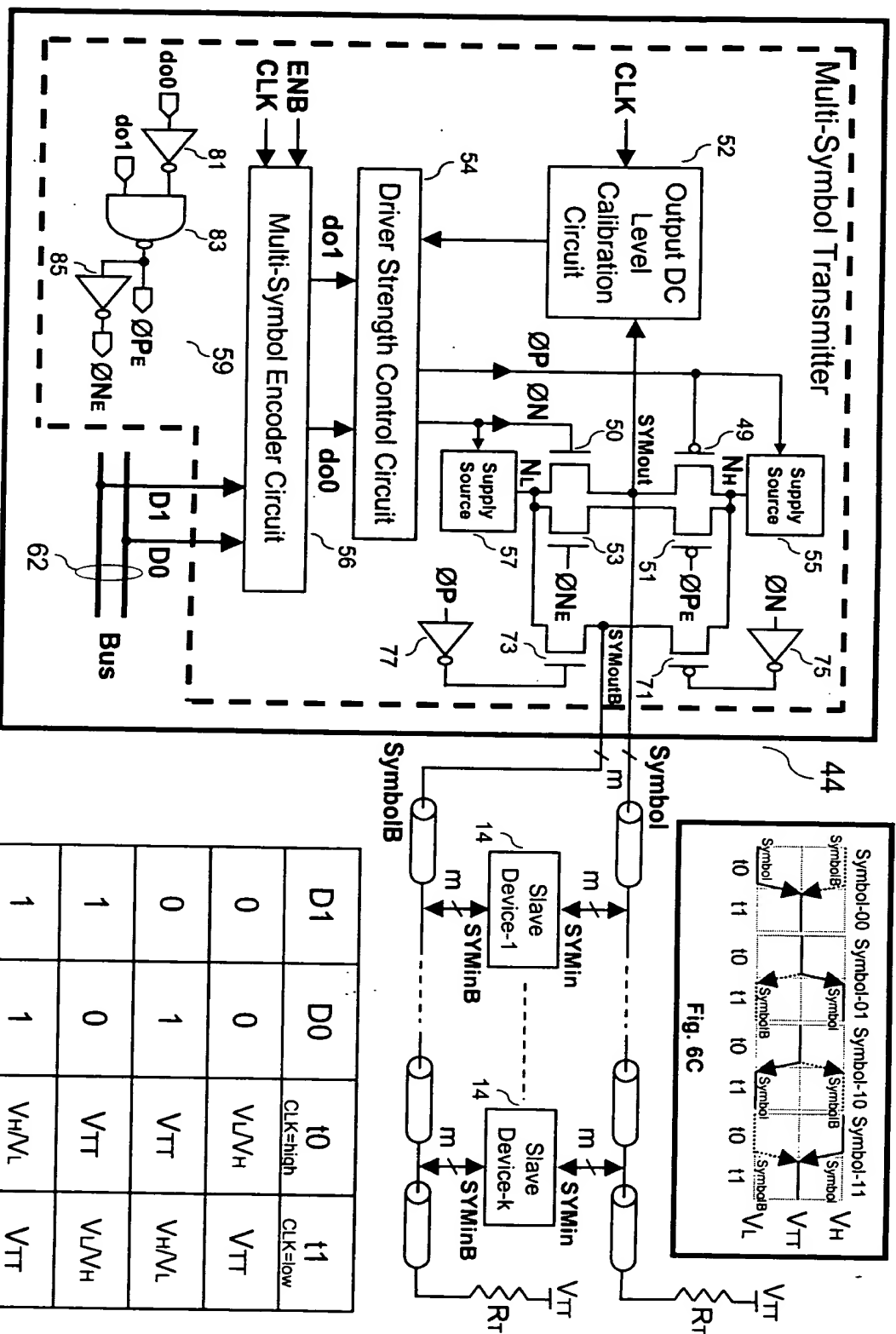
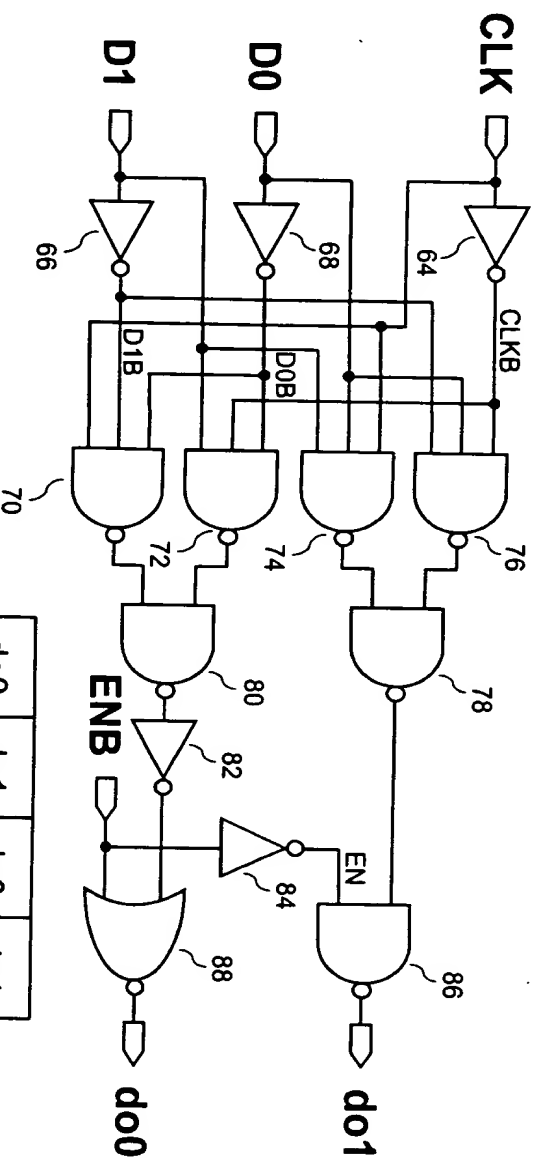


Fig. 6B

D1	D0	t0 CLK=high	t1 CLK=low
0	0	V <sub>L</sub> /V <sub>H</sub>	V <sub>TT</sub>
0	1	V <sub>TT</sub>	V <sub>H</sub> /V <sub>L</sub>
1	0	V <sub>TT</sub>	V <sub>L</sub> /V <sub>H</sub>
1	1	V <sub>H</sub> /V <sub>L</sub>	V <sub>TT</sub>

Symbol/  
Symbol  
Symbol/  
Symbol

# Multi-Symbol Encoder



				70			
				do0	do1	do0	do1
D1	D0	$t_0$ CLK=high	$t_1$ CLK=low	$t_0$ CLK=high	$t_0$ CLK=high	$t_1$ CLK=low	$t_1$ CLK=low
0	0	$V_L$	$V_{TT}$	1	1	0	1
0	1	$V_{TT}$	$V_H$	0	1	0	0
1	0	$V_{TT}$	$V_L$	0	1	1	1
1	1	$V_H$	$V_{TT}$	0	0	0	1

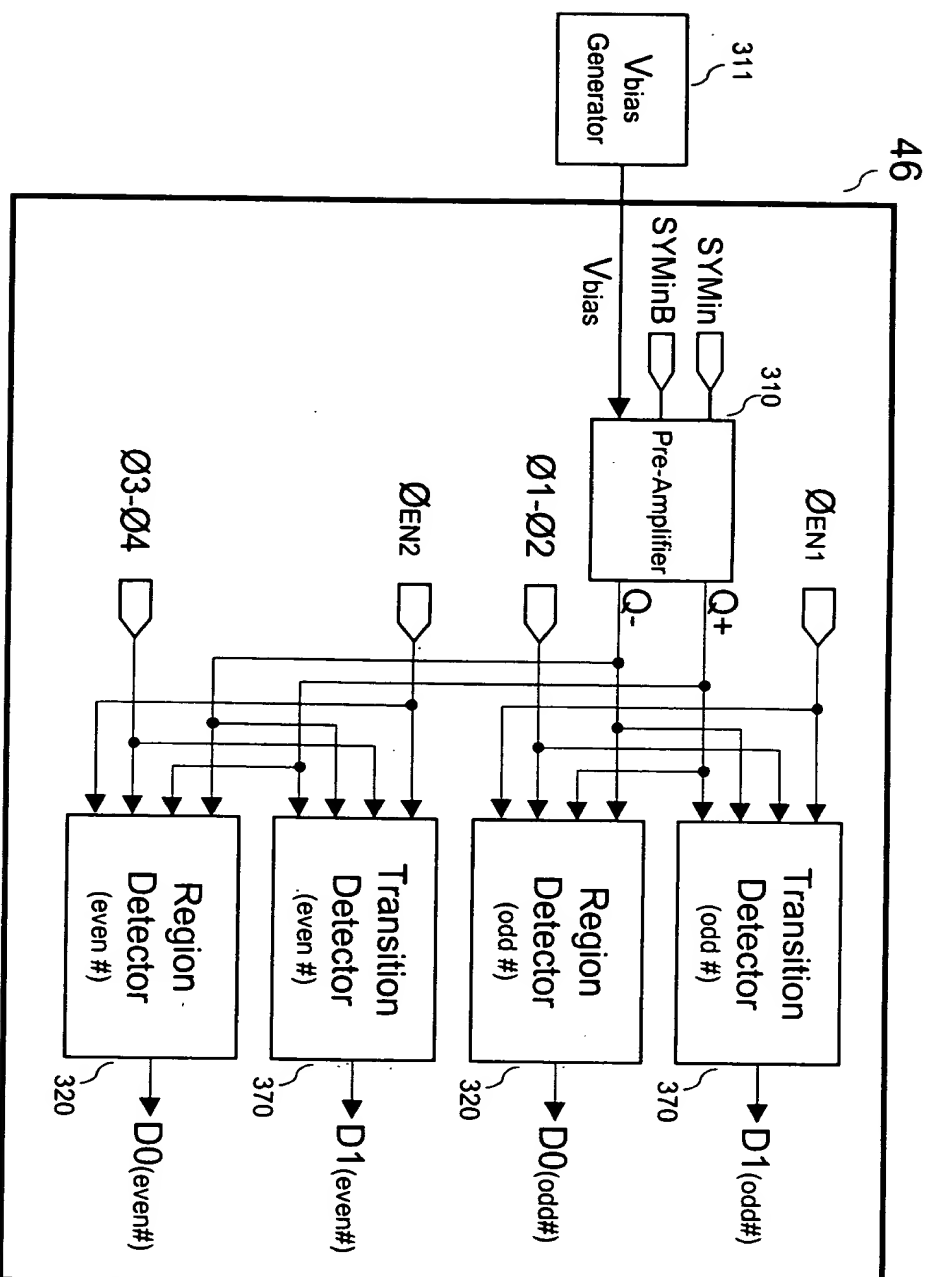
**Fig. 7**

[illegible]



[illegible]

# Multi-Symbol CMS Receiver



**Fig. 9**

# Pre-Amplifier

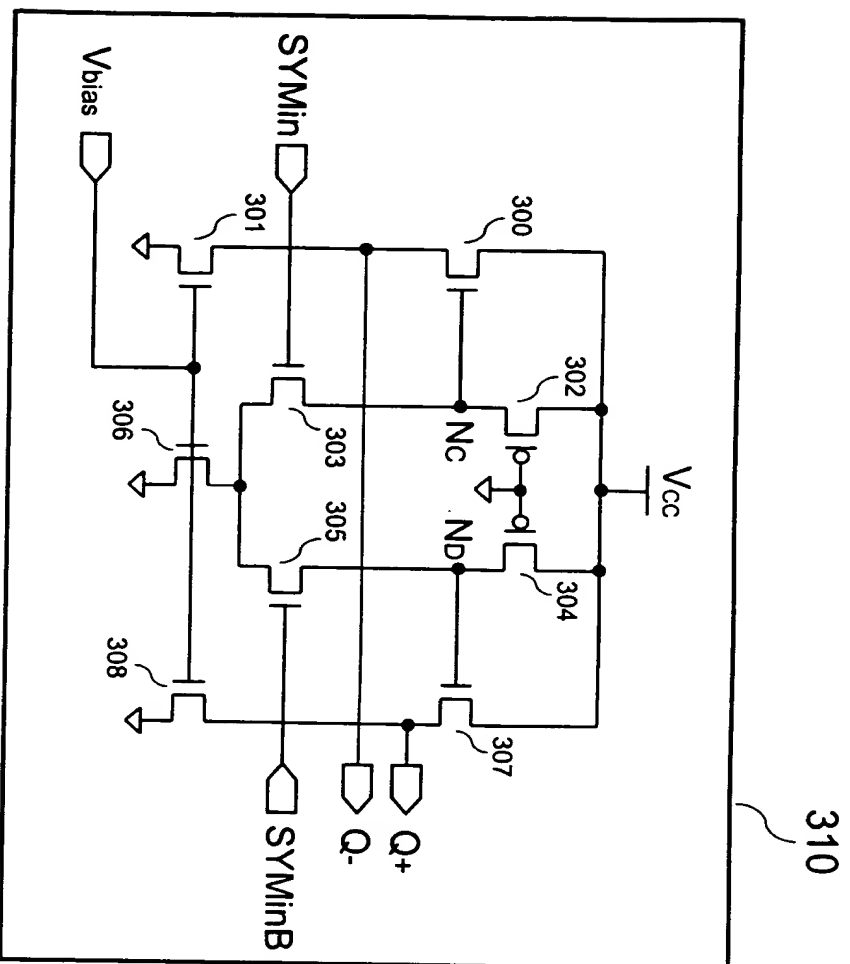
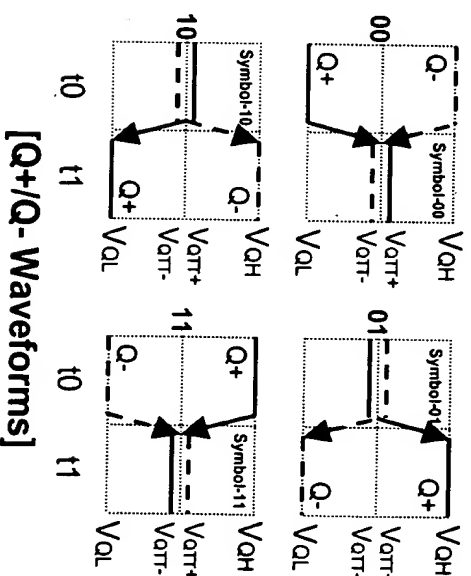
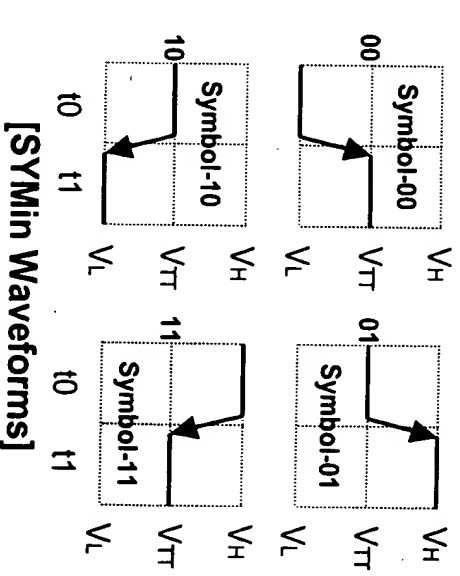


Fig. 10



# Transition Detector

Fig. 11A

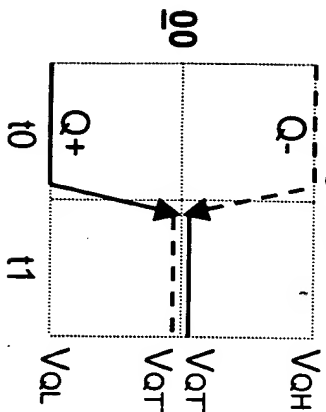


Fig. 11B

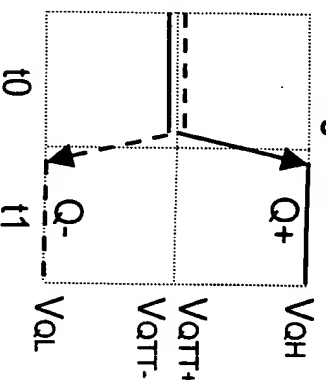


Fig. 11C

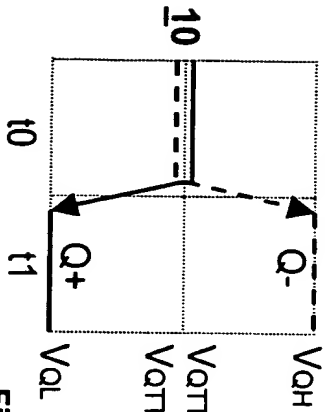


Fig. 11D

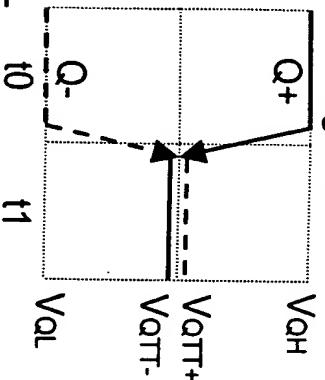


Fig. 11E

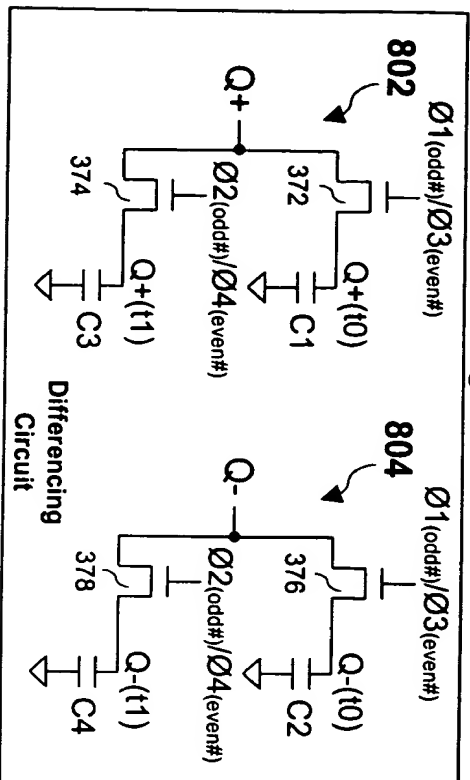


Fig. 11F

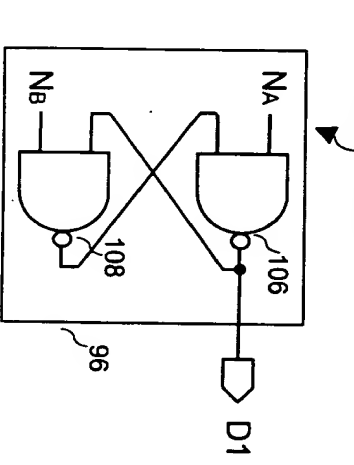
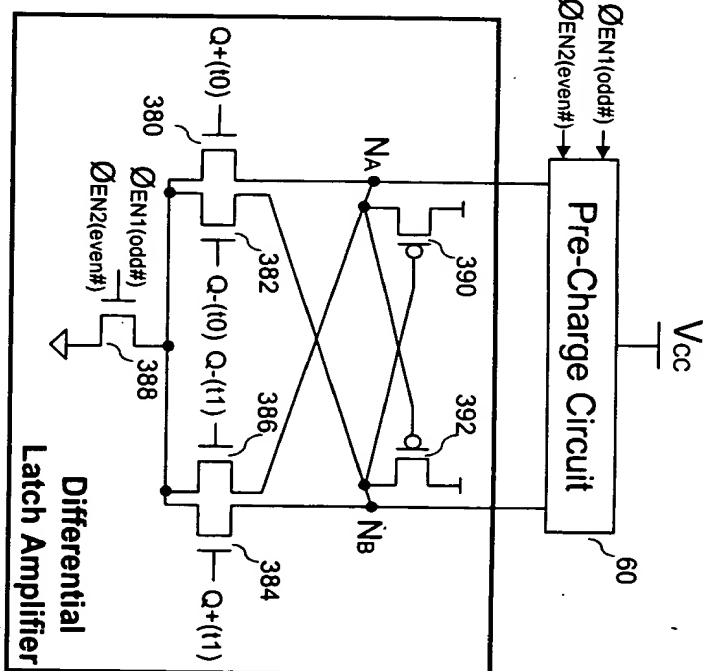


Fig. 11G



# Region Detector

Fig. 12A

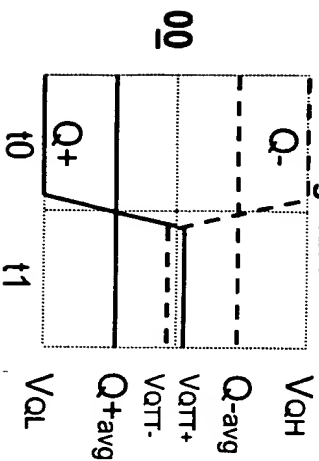


Fig. 12B

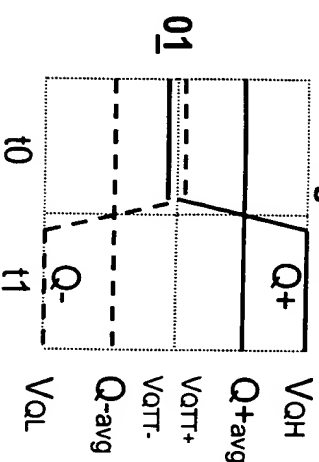


Fig. 12C

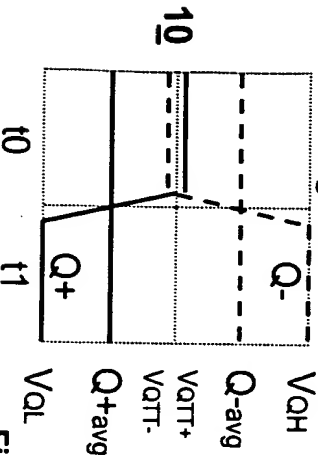


Fig. 12D

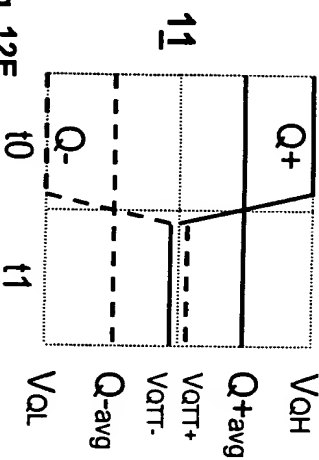


Fig. 12E

130

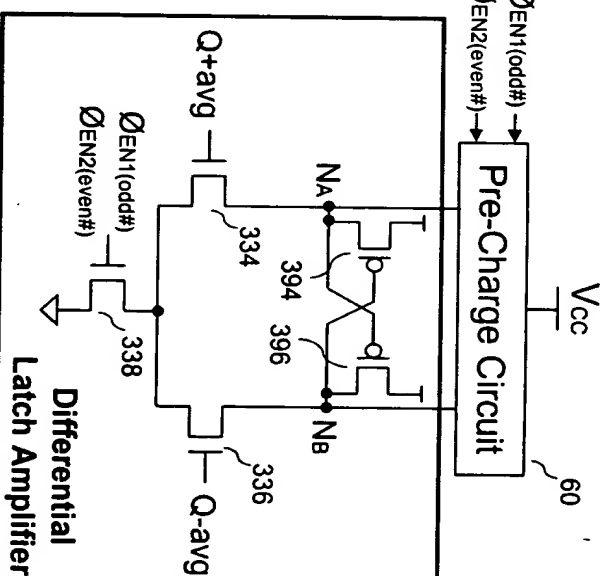
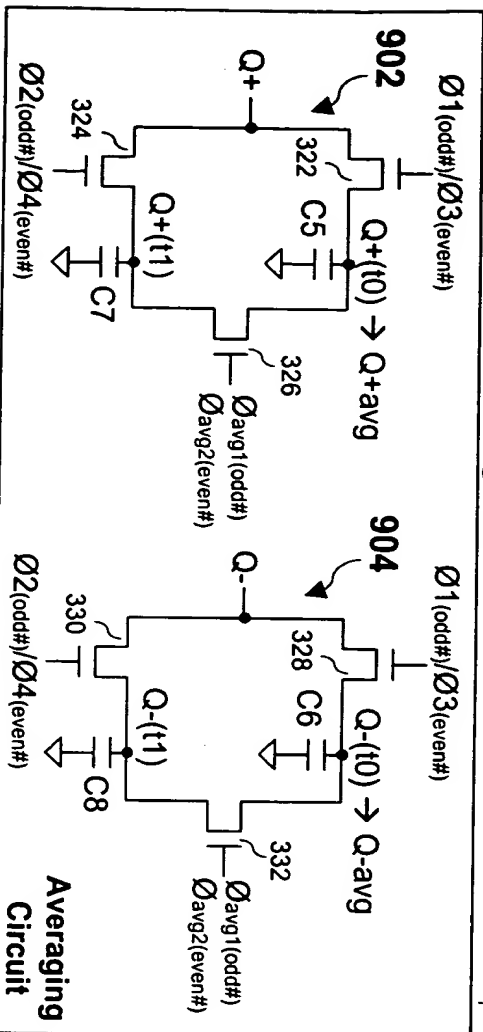


Fig. 12F

128



Averaging Circuit

Hold Circuit

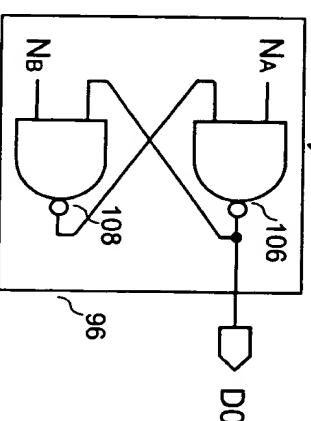


Fig. 12G

96

D0

# Pre-Charge Circuit

60

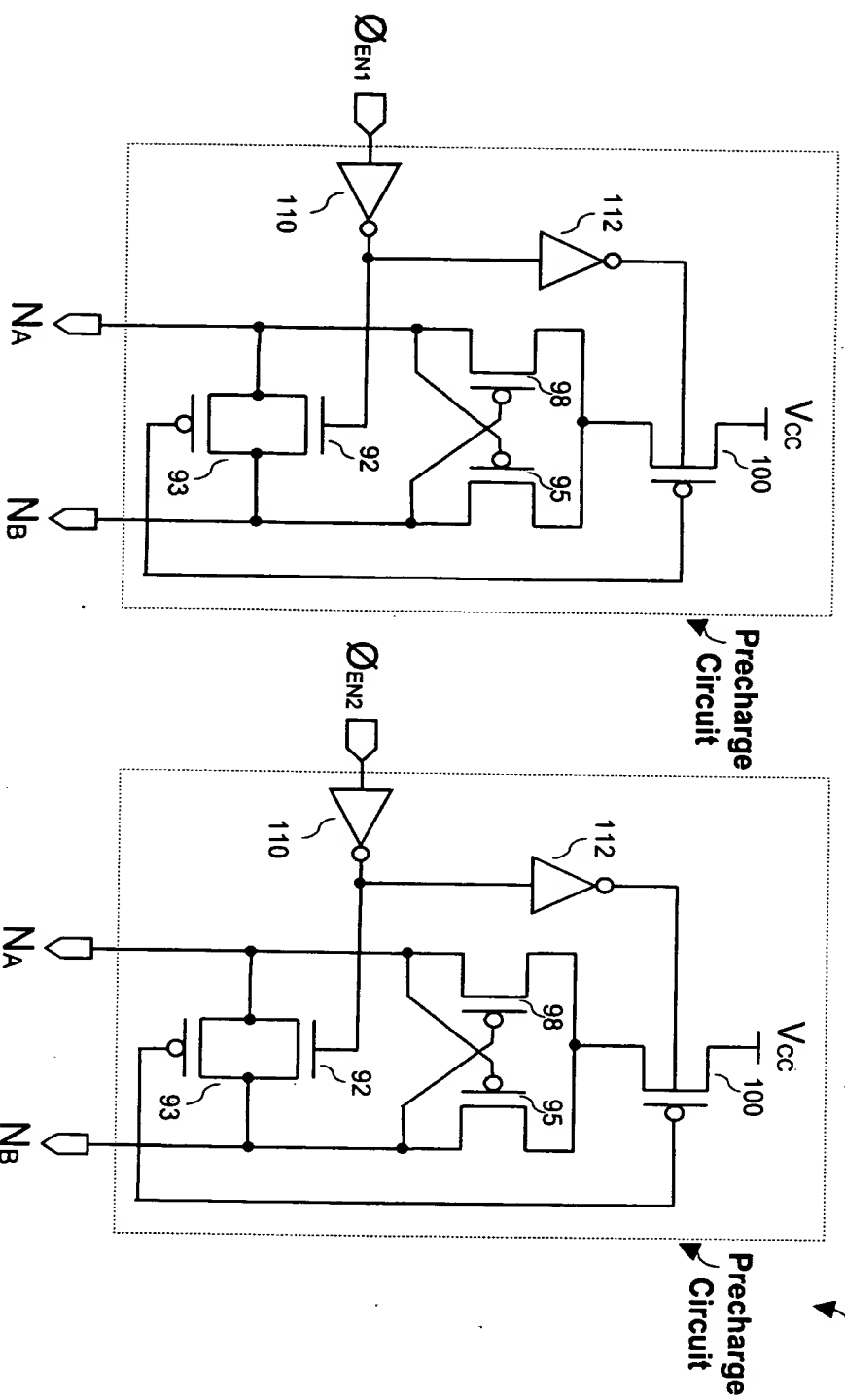


Fig. 13

# Multi-Symbol Transfer Control Timings

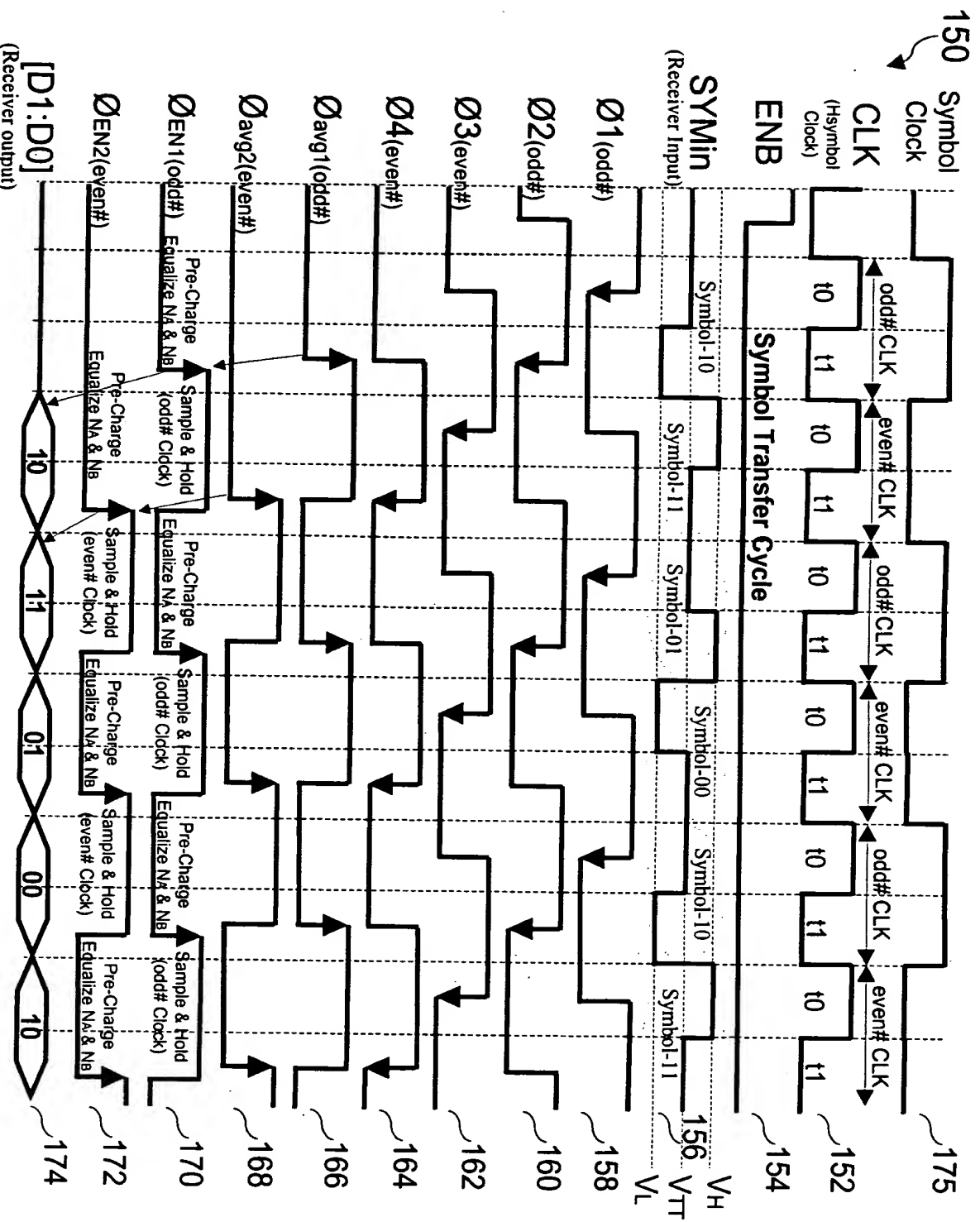


Fig. 14